

FIG. 1(a)

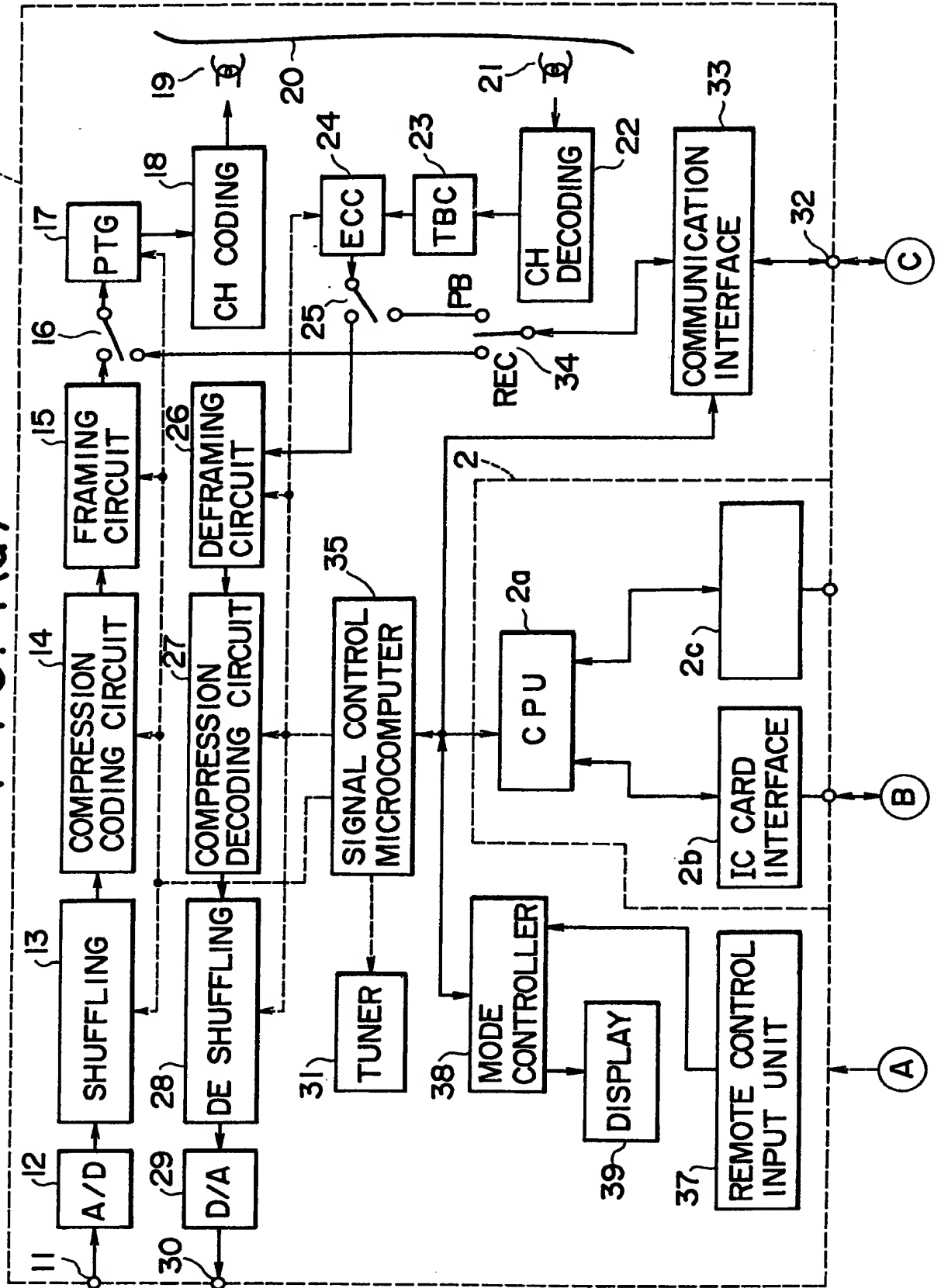


FIG. 1(b)

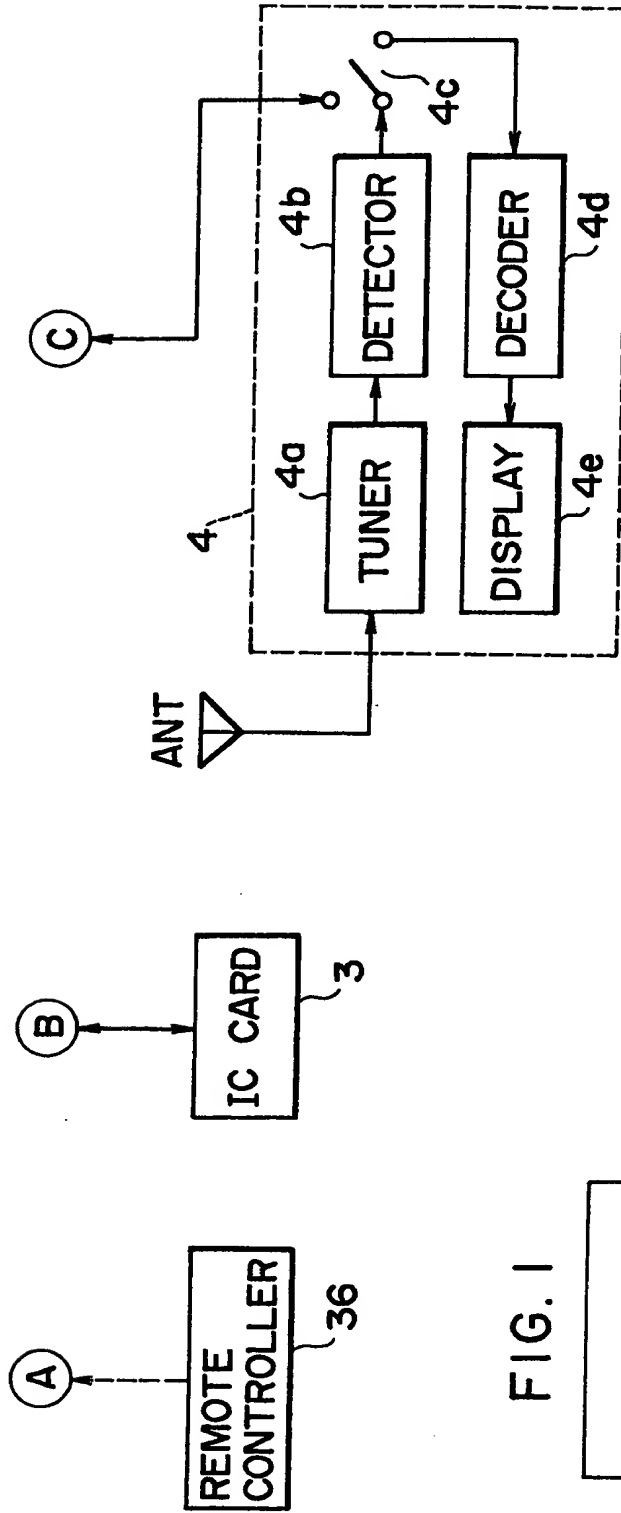
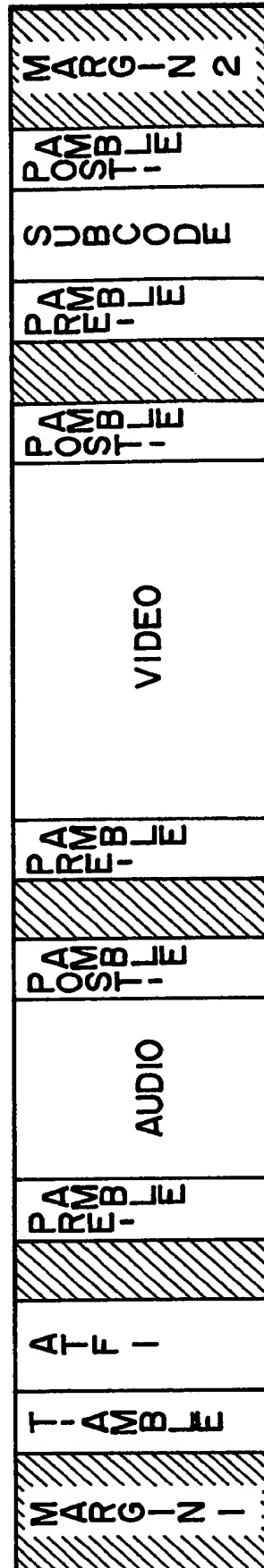


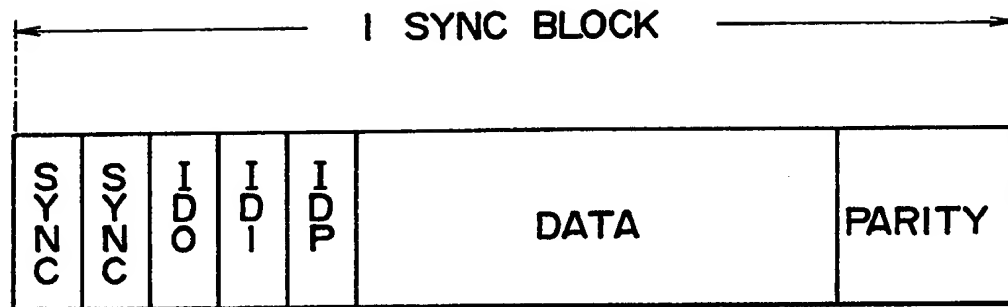
FIG. 1

FIG. 1(a)
FIG. 1(b)

FIG. 2



F I G. 3(a)



F I G. 3(b)

FRID	SYNC7
RESERVED	SYNC6
RTYPE I	SYNC5
RTYPE0	SYNC4
SYNC I I	SYNC3
SYNC I O	SYNC2
SYNC9	SYNC I
SYNC8	SYNC0

FIG. 4(a)

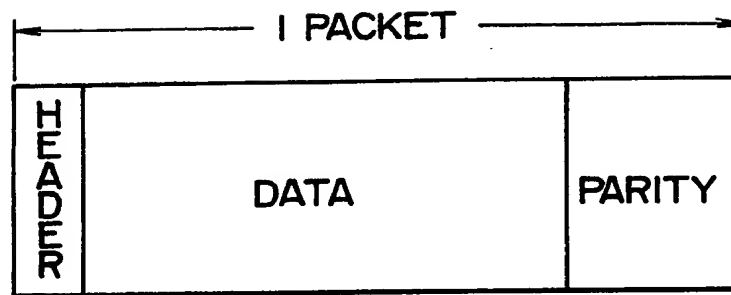


FIG. 4(b)

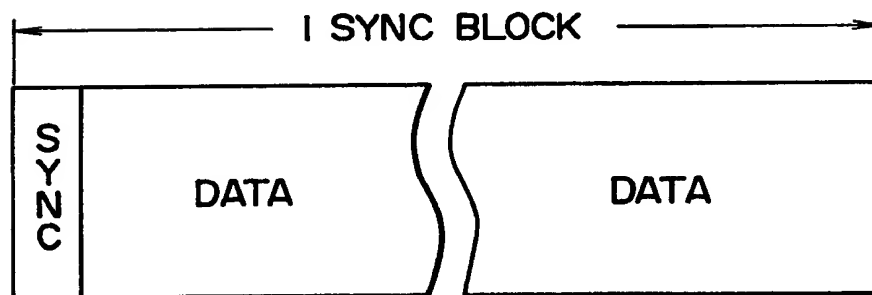


FIG. 5

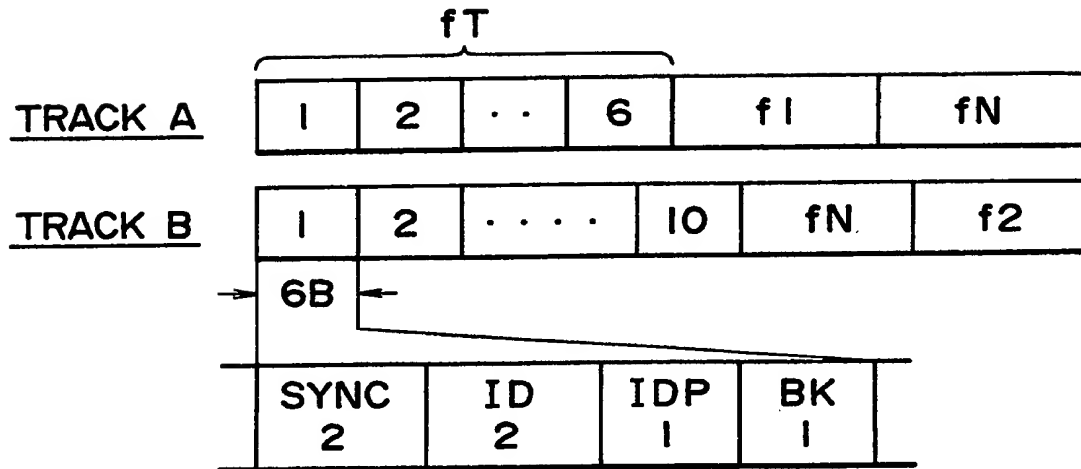
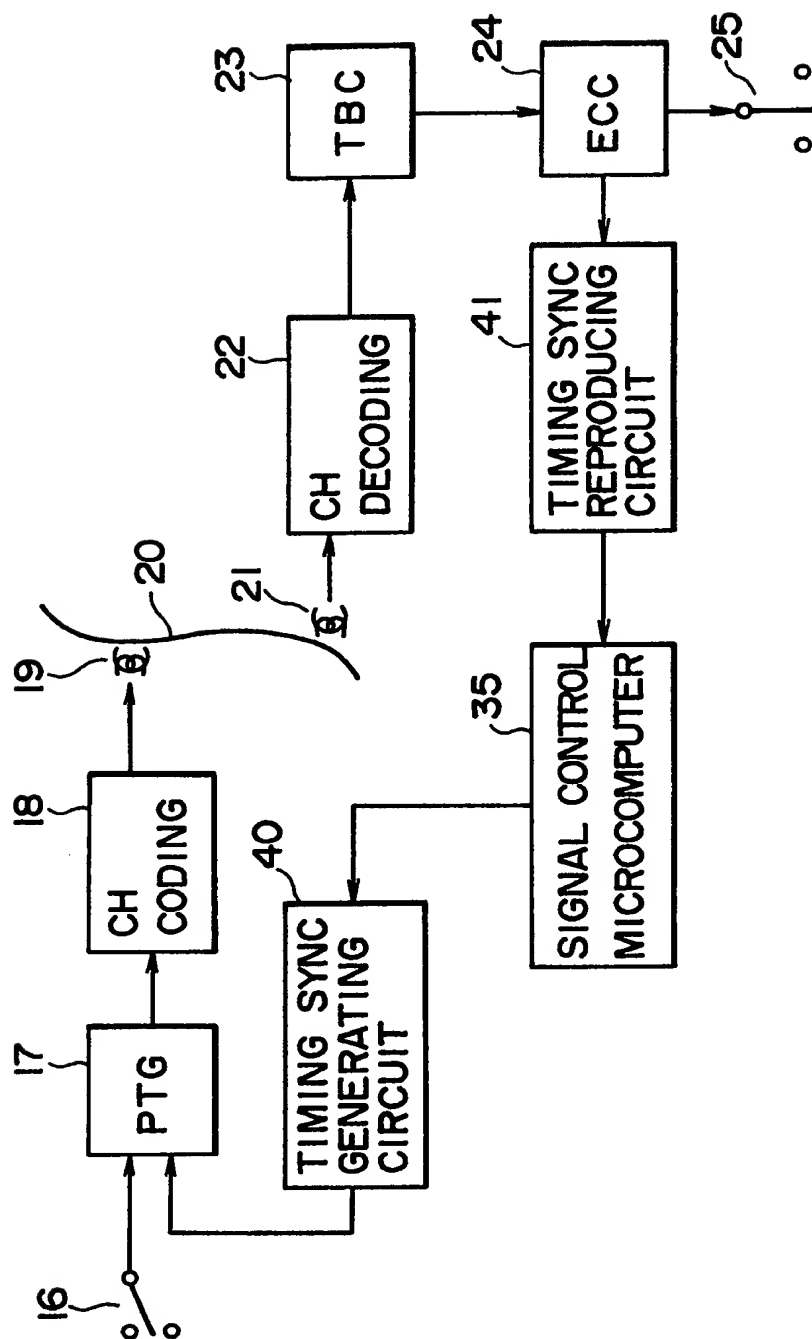


FIG. 6

SP/LP	RESERVED
FORMAT TYPE	RESERVED
RTYPE 1	RESERVED
RTYPE 0	SYNC 4
FORMAT TYPE	SYNC 3
FORMAT TYPE	SYNC 2
FORMAT TYPE	SYNC 1
RESERVED	SYNC 0

FIG. 7



**RECORDING AND/OR REPRODUCING DEVICE FOR DIGITAL SIGNAL
INCLUDING IC CARD READER**

5 The present invention relates to a digital video
signal recording and reproducing apparatus such as a digital
video cassette recorder (VCR) and, more particularly, to a
digital video signal recording and reproducing apparatus
incorporating an IC card reading/writing unit.

10 There have been put on the market various types of
analog VCRs for use in the home. Although a home digital VCR
has not yet been marketed, there are a number of examples that
underwent trial manufacture and these are identified by Y. Eto,
et al. in "Digital Video Recording Technology", p. 158.

15 Since the above-described analog VCRs and digital
VCRs have their circuits arranged to record and reproduce video
signals in the existing formats, in the event that a video
signal in a new format is employed, they cannot record and
reproduce the signal unless additional circuits supporting the
new format are attached to them. Further, such VCRs are unable
20 to perform operations other than recording and reproducing
video signals.

Accordingly, it is an object of the present invention
to solve such problems as described above and, specifically,
it is an object of the present invention to provide a digital
25 video signal recording and reproducing apparatus capable of
recording and reproducing signals in future formats without the
need for attaching new circuits thereto.

It is another object of the present invention to
provide a digital video signal recording and reproducing
30 apparatus which can also be used as a terminal unit for IC card
application systems. Thus, the present invention in one aspect
provides a digital video signal recording and reproducing
apparatus with an IC card reader/writer.

In one embodiment of the present invention the IC
35 card stores control data corresponding to the transmission

format of a recorded video signal. Such an IC card is loaded into the IC card reader/writer incorporated in the digital video signal recording and reproducing apparatus and, thereby, the signal processing circuits in the digital video signal recording and reproducing apparatus are controlled. The signal processing circuits in the digital video signal recording and reproducing apparatus are structured of digital signal processors (DSPs), and the circuits are controlled in operation such that the sync block length of record data or the track pattern is changed by the control data stored in the IC card.

Further, in the reproduction mode an IC card storing control data corresponding to the transmission format of the reproduced digital signal is used and the signal processing circuits in the reproducing system are controlled in response to this control data.

In another embodiment, the present invention also provides recording, in the ATF area, of data corresponding to the transmission format of the recorded signal and, by reproducing the data, provides control of the signal processing circuits in the reproducing system in accordance with the data.

In addition, a compression coding circuit can be formed of a digital signal processor and a compression coding system can be set up using an IC card storing control data corresponding to the compression coding system.

Also, the selection frequency of an integrated tuner can be controlled by the use of an IC card. Further, a scramble decoder can be controlled by the use of an IC card storing control data capable of descrambling scrambled signals that are either received or recorded.

Still further, by employing a host interface to the IC card reader/writer the digital video signal recording and reproducing apparatus can be used as a terminal unit for IC card application systems such as home banking, home trade, home shopping, home reservations and so on.

According to the present invention, by loading an IC

card storing specific control data into an IC card reader/writer incorporated in a digital video signal recording and reproducing apparatus, operational control and the like of the signal processing circuits of the recording and reproducing system, the selection frequency of the tuner, the format of the scramble decoder, and so on can be achieved. Further, the apparatus can also be used as a terminal unit for an IC card application system.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings, in which:-

FIG. 1 is a block diagram schematically showing the structure of a digital VCR according to an embodiment of the present invention;

FIG. 2 is a diagram showing a data arrangement recorded on one track in the digital VCR according to an embodiment of the invention;

FIGS. 3(a) and 3(b) are diagrams showing a format and ID in the record data in an embodiment of the invention;

FIGS. 4(a) and 4(b) are diagrams showing a digital broadcast format;

FIG. 5 is a diagram showing the timing sync and ATF pilot signals in a digital VCR according to an embodiment of the invention;

FIG. 6 is a diagram showing an example of ID data recorded in the timing sync in an embodiment of the invention; and

FIG. 7 is a block diagram showing a structure for processing various types of ID data shown in FIG. 6.

Referring to FIG. 1, an analog video signal input at a terminal 11 of a digital VCR 1 is converted to a digital video signal by an A/D converter circuit 12. The digital video signal data then undergoes a change in order by a shuffling circuit 13 as well as undergoing discrete cosine transformation and variable length encoding in a compression coding circuit

14. Output of the compression coding circuit 14 is arranged into a format code structure in a framing circuit 15 and is supplied to a parity generating circuit 17 through a switching circuit 16. In the parity generating circuit 17, the signal is given parity, synchronization code, and ID data and is then supplied to a channel coding circuit 18. The signal is subjected therein to parallel/serial conversion and conversion to a record code, and then is recorded on a magnetic tape 20 by a recording head 19. On the magnetic tape 20, the digital video signal for one frame, together with the digital audio signal, subcode signal, ATF pilot signal, and others are recorded as a plurality of oblique tracks, for example, 10 tracks in the NTSC system, 20 tracks in the HDTV system. The recording head 19 is formed, for example, of a pair of heads having different azimuth angles and disposed at an interval of 180° on a rotating drum. Processing systems for the audio signal, subcode signal, and ATF signal are not shown, because the use of such systems are well known.

A digital video signal reproduced from the magnetic tape 20 by a playback head 21 is subjected to decoding of the record code and serial/parallel conversion in a channel decoding circuit 22 and is subjected to time base correction in a time base corrector 23. The output of the time base corrector 23 is subjected to error correction processing with the use of product code in an Error Correcting Coding (ECC) circuit 24 and is supplied to a deframing circuit 26 through a switching circuit 25. The signal supplied to the deframing circuit 26 is converted therein to variable length coded data, which is then subjected to decoding of the variable length code and inverse discrete cosine conversion in a compression decoding circuit 27. The signal is then restored to data in the original order in a deshuffling circuit 28, converted to an analog video signal in a D/A converter 29, and output at terminal 30.

In this embodiment, the circuits in the recording

system from the shuffling circuit 13 to the parity generating circuit 17 and the circuits in the reproduction system from the ECC circuit 24 to the deshuffling circuit 28 are formed of DSPs and are controlled by a signal control microcomputer 35 to operate under optimum conditions. The details of this DSP control by the control microcomputer will be described below.

A remote controller 36 is used for setting operational modes, such as ON/OFF, Record, Play, Fast Forward, Record Timer, of the digital VCR 1. The signal specifying the operational mode transmitted from the remote controller 36 is supplied from a remote control input unit 37 to a mode controller 38. The mode controller 38 detects the input operational mode and outputs the appropriate control signal to the pertinent part. A display 39 displays the operational mode. The remote control 36 is used as a key pad when the digital VCR 1 is used as a terminal unit for an IC card application system. The output of the mode controller 38 is also supplied to a CPU 2a of an IC card reader/writer 2.

FIG. 2 shows an example of a data arrangement recorded on one track of a digital VCR according to an embodiment of the present invention. The example shown is a data arrangement of a recorded digital video signal, in which the left end of the track is the input side to the head and the right end is the output side, that is, the track is shown travelling from left to right in relation to the head.

In preamble and postamble areas, disposed on both ends of the data record area, there is recorded a pulse signal, with the same frequency as the bit frequency of the data, to be used for reproduction of the clock by means of a PLL. Data are not recorded in margin areas or in inter block gaps (IBG), which are shown shaded in Fig, 2. At left and right ends of the track there are provided a margin 1 and a margin 2, respectively. Next to the margin there is disposed a Track-amble or T-amble and then a first automatic tracking frequency (ATF) area, ATF 1, in which an ATF pilot signal and a timing

sync are recorded. There are disposed then, from left to right in FIG. 2, record areas of the digital audio signal, the digital video signal, and the subcode signal.

FIGS. 3(a) and 3(b) are diagrams showing examples of the format of record data and ID data in this embodiment of the invention. As shown in FIG. 3(a), there are disposed two bytes of sync codes and three bytes of IDs, one byte of which is ID parity, in front of each block data of predetermined length, which is followed by a parity code. The format is formed in the framing circuit 15 or the parity generating circuit 17 in FIG. 1. The data length and parity are set when a television signal is recorded, for example, in the pattern shown in FIG. 2, such that the digital video signal has 77 bytes for data and 8 bytes for parity, the digital audio signal has 77 bytes for data and 8 bytes for parity, and the subcode signal has 5 bytes for data and 2 bytes for parity.

When a television signal is recorded in the pattern shown in FIG. 2, the ID data of FIG. 3(b) in two bytes is defined as follows:

- (a) the most significant bit of the first byte: frame ID;
- (b) the seventh bit of the first byte: reserved;
- (c) the sixth and fifth bits of the first byte: identification of the record data, that is video, audio, or subcode;
- (d) the first to fourth bits of the first byte: sync block numbers;
- (e) the most significant bit to the first bit of the second byte: sync block numbers.

Further, it may be well to record data identifying the format of the recorded television signal, such as NTSC, PAL, HD, wide vision, using one byte of the record data portion.

The case where an analog video signal input at the terminal 11 is recorded has been described above. The analog

video signal input at terminal 11 may be a video signal generated by an external video camera (not shown), a video signal output from a tuner 31 incorporated in the VCR 1, or the like. The digital VCR 1 can also record a signal of digital
5 broadcasting, streamer, or the like input from a digital I/O port 32. The apparatus shown in FIG. 1 is adapted to record a signal of digital broadcasting received by an external digital broadcasting picture receiver 4. Operation in such a case will be described below.

10 An electromagnetic wave carrying digital broadcasting received by an antenna ANT is input to the digital broadcasting picture receiver 4. The signal of the digital broadcasting is compression coded on the transmission side according to a predetermined algorithm. From the signal of the digital
15 broadcasting input to the digital broadcasting picture receiver 4, a signal of a desired channel is selected by a tuner 4a and the signal is converted to a bit stream signal by a detector 4b.

20 When it is desired to see the bit stream signal, the switching circuit 4c is switched over to the side of a decoder 4d and the signal is compression decoded in the decoder 4d and displayed on a display unit 4e. When it is desired to record the signal in the digital VCR 1, the switching circuit 4c is
25 switched over to the side of the external output and the signal is supplied to the digital I/O port 32 of the digital VCR 1.

The bit stream signal input from the digital I/O port 32 to a communication interface 33 is input to the parity generating circuit 17 through a switching circuit 34 and the switching circuit 16. The record processing thereafter is the
30 same as with an analog video signal input at the terminal 11. Also, the processing in this reproduction operation is the same as that in the ordinary reproduction operation up to the stage where error correcting processing is performed with the product code in the ECC circuit 24.

35 The output of the ECC circuit 24 is input to the

digital broadcasting picture receiver 4 through the switching circuit 25, switching circuit 34, communication interface 33, and the digital I/O port 32. The signal is fed from the switching circuit 4c to the decoder 4d to be compression
5 decoded therein and then displayed on the display unit 4e.

The bit stream signal of the digital broadcasting has compressed data of a predetermined length has a header at the front and a parity word at the rear, as shown in FIG. 4(a) and, thereby, forms one packet. Alternately, it is arranged in a
10 format of a sync block having a predetermined length, which can be one frame, of data with a sync code at the front, as shown in FIG. 4(b). If the parity generating circuit 17 or the ECC circuit 24 is so structured that the record data length and the like shown in FIG. 3(a) have fixed values, digital broadcasting
15 will not be supported by them in the event that digital broadcasting in new transmission formats having different packet lengths or different sync block lengths is used in the future.

Accordingly, in this embodiment, the parity
20 generating circuit 17 and the ECC circuit 24 are structured of DSPs and are adapted such that a format in which such parameters as the record data length are changed can be set up easily in accordance with control data corresponding to a transmission format of digital broadcasting stored in an IC
25 card 3. The IC card 3 is provided with CPU, ROM, RAM, and EPROM. The control data corresponding to the transmission format of digital broadcasting stored in the EPROM is input from an IC card interface 2b of the IC card reader/writer 2. The CPU 2a identifies the content of the data and supplies it
30 to the signal control microcomputer 35. The signal control microcomputer 35 controls the parity generating circuit 17 and the ECC circuit 24 to process data in the format corresponding to the transmission format of the digital broadcasting. When digital broadcasting in some new transmission format is used
35 in the future, an IC card corresponding to the transmission

format can be produced and utilized in the present invention to process data in such new format.

It is desired here that the record data length is set to be an integral multiple or an integral submultiple of the packet length in digital broadcasting. Alternatively, it is desired to be an integral submultiple of the sync block length of digital broadcasting. If such a setting is so made, reproduction of data becomes easy even when changed-speed reproduction is performed at the time of Cue/Review or the like.

According to the digital VCR of this embodiment as described above, the parity generating circuit 17 and the ECC circuit 24 are structured such that they can freely change the data length of record data. Therefore, even when the format of digital broadcasting is changed or a new format appears in the future, the signal of the digital broadcasting in the new format can then be recorded by using an IC card storing control data corresponding to the new format.

While operations in the case where an IC card storing control data corresponding to a transmission format of digital broadcasting have been described above, the digital VCR is also capable of recording and reproducing a streamer input from the digital I/O port. In this case, the data length of one sync block shown in FIG. 3(a) is set to an optimal length corresponding to the streamer and the track pattern shown in FIG. 2 is changed to a pattern suited to the streamer. For example, the pattern may be changed so that the divisions of audio, video, and subcode, as well as the IBGs and amble areas provided therebetween are eliminated.

In the ATF area of the track of data, referred to as "format type", which identifies the kind of record data such as digital broadcasting, streamer, and its parameters such as data length, sync block length, is recorded.

FIG. 5 is a diagram showing the timing of the digital VCR and the ATF pilot signal according to an embodiment of the

invention. In the track A, six blocks of timing sync fT are recorded from the head and then a first pilot signal of frequency f1 and a Nyquist frequency fN are recorded. In the track B, 10 blocks of timing sync are recorded from the head and then Nyquist frequency fN and a second pilot signal of frequency f2 are recorded. This is the pattern of the SP mode which differs somewhat from that of the LP mode.

As described above, the timing sync is recorded in the ATF area at portions where the first and second pilot signals are not recorded. The tracks shown are those recorded by recording heads having mutually different azimuth angles. Description as to details of the pilot signal and the ATF control will be omitted because it is not directly related to the substance of the present invention.

As shown in FIG. 5, the timing sync having a sync block structure of six-byte length includes two bytes of synchronous code, two bytes of ID signal, one byte of parity IDP for error correction of the ID signal, and one byte of vacant area. When a television signal is recorded in the pattern shown in FIG. 2, the ID signal of two bytes in the timing sync is as shown in FIG. 6 as:

- (a) the most significant bit of the first byte: discrimination between SP/LP;
- (b) the seventh bit of the first byte: format type;
- (c) the sixth and fifth bits of the first byte: record data, that is, identification of its timing sync;
- (d) the fourth to second bit of the first byte: format type;
- (e) the least significant bit of the first byte: reserved;
- (f) the most significant bit to the sixth bit of the second byte: reserved;
- (g) the fifth bit to least significant bit of the second byte: sync block number.

FIG. 7 is a block diagram showing a structure for processing various types of the ID data shown in FIG. 6. Parts therein corresponding to those shown in FIG. 1 are denoted by the same reference numerals.

5 The timing sync generating circuit 40 is controlled by the signal control microcomputer 35 and generates the timing sync as shown in FIG. 5. At this time, as shown in FIG. 6, the format type corresponding to the control data in the four bits of ID of two bytes in the timing sync is set up. The output
10 of the timing sync generating circuit 40 is supplied to the parity generating circuit 17, passed through the channel coding circuit 18, and recorded by the recording head 19 on the magnetic tape 20.

 In the reproduction operation, the recorded signal
15 is reproduced by the reproduce head 21 from the magnetic tape 20 and supplied to the timing sync reproducing circuit 41 through the channel coding circuit 22, the time base corrector 23, and the ECC 24. The timing sync reproducing circuit 41 reproduces the timing sync and supplies it to the signal
20 control microcomputer 35. The signal control microcomputer 35 controls the ECC circuit 24 according to the format type set up in the four bits of the ID. Thus, by having the data identifying the format recorded on the tape, the data can be utilized in the reproduction operation.

25 In addition to the above described operations, the digital VCR according to the present invention can be made to perform the following operations by using an IC card:

 (a) Using an IC card storing control data corresponding to the transmission format of the digital signal
30 recorded on the magnetic tape for controlling the signal processing circuits in the reproducing system in response to the control data.

 (b) The digital VCR can be utilized as a terminal unit for an IC card application system. For example, the host
35 interface 2c can be connected to a modem and this modem

connected through the public network to a host computer in a bank, a stock brokerage, a department store, or an airline. Then, by using an IC card issued by such company, home banking, home trade, home shopping, home reservation, and so on can be made. Since the remote controller 36 belonging to the digital VCR 1 is provided with various operation keys such as numeric keys, a dedicated key pad for carrying out such a banking, shopping, or reservation procedure becomes unnecessary and the IC card reader/writer needs no additional key pad interface. Further, the television picture receiver or monitor device connected to the digital VCR 1 or an LCD display provided on the remote controller 36 can be utilized as a display unit to be used in the above procedures.

(c) Using an IC card storing control data corresponding to the kind of recorded signal, for example, HDTV or SDTV, and/or the record mode, for example SP or LP, the algorithm for the shuffling circuit 13, compression coding circuit 14, and framing circuit 15, all comprised of DSPs, can easily be set up. In addition, the number of revolutions of the rotating head drum or the travelling speed of the magnetic tape may be set up by the control data stored in the IC card.

(d) By using an IC card to control the deframing circuit 26, compression decoding circuit 27, and deshuffling circuit 28, all composed of DSPs, reproduced signals of digital broadcast data which have been compressed using various algorithms can be decoded.

(e) Using an IC card the selection frequency of the incorporated tuner 31 can be controlled. Thus, even when the number of reception frequencies is increased in the future, the selection frequency can be controlled with an IC card.

(f) By providing a scramble decoder and using an IC card storing control data to achieve descrambling, the scramble decoder can be controlled.

According to the present invention as described above, when it is desired to record transmission formats, such

as digital broadcasting, streamer, and the like, to which are not yet utilized but which will appear in the future, such formats can be supported by an existing digital video signal recording and reproducing apparatus by using an IC card storing control data for the signal processing circuits corresponding to each new format.

Further, by means of the incorporated IC card reader/writer, the apparatus can be used as a terminal unit for an IC card application system and hence, the use of the digital video signal recording and reproducing apparatus can be expanded.

Finally, it must be noted that although the present invention is described by reference to particular embodiments thereof, many changes and modifications of the invention may become apparent those skilled in the art without departing from the spirit and scope of the invention, which is only limited by the appended claims.

CLAIMS

1. A recording and/or reproducing apparatus for a digital video signal comprising:
5 a video signal recording and/or reproducing unit having controllable digital signal processing circuits;
an IC card reading and/or writing unit integrated into the video signal recording and/or reproducing unit and connected to said digital signal processing circuits; and
10 an IC card storing control data for reading by said IC card reading and/or writing unit and controlling said digital signal processing circuits.
2. The recording and/or reproducing apparatus according to claim 1, wherein said control data corresponds to a transmission format of said digital video signal.
3. The recording and/or reproducing apparatus according to claim 2, wherein said control data corresponds to a record track pattern of said digital video signal.
4. The recording and/or reproducing apparatus according to claim 2, wherein said control data corresponds to a sync block length of said digital video signal.
- 25 5. The recording and/or reproducing apparatus according to claims 2, 3, or 4, wherein said video signal recording and/or reproducing unit records data corresponding to the transmission format of said digital video signal in an automatic tracking frequency area of a track on a record medium.
- 30 6. The recording and/or reproducing apparatus according to claims 2, 3, or 4, wherein said video signal recording and/or reproducing unit reproduces said digital video signal
- 35

in accordance with said control data corresponding to the transmission format of said digital video signal.

5 7. The recording and/or reproducing apparatus according to any one of the preceding claims, wherein one of said digital signal processing circuits comprises a compression coding circuit for setting up a compression coding format responsive to said control data.

10 8. The recording and/or reproducing apparatus according to any one of the preceding claims, wherein said video signal recording and/or reproducing unit further comprises an integrated tuner, and wherein a selection frequency of said tuner is controlled by said control data.

15 9. The recording and/or reproducing apparatus according to any one of the preceding claims, wherein said video signal recording and/or reproducing unit further comprises an integrated scramble decoder controlled by said control data,
20 whereby the control data causes the video signal recording and/or reproducing unit to descramble a scrambled digital video signal.

25 10. The recording and/or reproducing apparatus according to any one of the preceding claims, wherein said video signal recording and/or reproducing unit further comprises interface means for interfacing for connecting said video signal recording and/or reproducing unit to an information transmission network, whereby said video signal recording
30 and/or reproducing unit functions as an IC card terminal unit.

35 11. A recording and/or reproducing apparatus constructed and arranged to operate substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

12. Supply of an IC card to permit a video record medium to have video information written thereon or read therefrom according to a particular video format by the apparatus of claim 1 by conditioning the apparatus to process video signals in accordance with that format."
- 5

Relevant Technical Fields

- (i) UK Cl (Ed.M) H4F (FDC, FEH, FJF, FGXX); G5R (RHC, RHX); H3P (QCD); G3N (NG1A4, NG1B)
- (ii) Int Cl (Ed.5) H04N (5/76, 5/78, 5/781, 5/782, 5/783, 5/91, 5/92, 5/93, 9/64, 9/79, 9/80, 9/87)

Databases (see below)

(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) WPI ONLINE

Search Examiner
M J DIXON

Date of completion of Search
12 JANUARY 1994

Documents considered relevant following a search in respect of Claims :-
ALL

Categories of documents

- | | |
|--|---|
| <p>X: Document indicating lack of novelty or of inventive step.</p> <p>Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.</p> <p>A: Document indicating technological background and/or state of the art.</p> | <p>P: Document published on or after the declared priority date but before the filing date of the present application.</p> <p>E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.</p> <p>&: Member of the same patent family; corresponding document.</p> |
|--|---|

Category	Identity of document and relevant passages	Relevant to claim(s)
X	WO 85/04989 A (ITV TELEVISION & VIDEO-SYSTEME) See Figure 1 and also WPI abstract accession number 85-289739/46	1, 2, 6

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